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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,359	09/24/2003	Hiroshi Miura	103213-00057	4693

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EXAMINER	
SORRELL, ERON J	
ART UNIT	PAPER NUMBER
2182	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/29/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/668,359	MIURA ET AL.	
	Examiner	Art Unit	
	Eron J. Sorrell	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *1 and 4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3 and 5-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/1/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 2,5, and 7-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claims 2 and 5 recites "a register for permitting a CPU to make DMA transfer, therein…" This limitation is unclear to the Examiner. It appears as if there is language missing. A CPU normally does not perform DMA rather initializes registers for setting up a DMA transfer. It is also unclear what is meant by "an occurrence of data storage in the first register." In the interest of compact prosecution, claim 2 and claims depending therefrom will be examined has best understood by the Examiner, however, appropriate correction is required.

4. Claims 7-9 are rejected based on their dependency to claim

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 2,5, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Taniai et al. (U.S. Patent No. 5,438,665 hereinafter "Taniai").

7. Referring to claims 2 and 5, Taniai teaches a data processing apparatus (figure 1) comprising a CPU (see item 10, figure 1) for executing a program and a memory (item 14, figure 1) for storing data or for storing data and the program wherein the data can be read out from the memory through a DMA controller (item 11, figure 1), the DMA controller (see figure 2 for block diagram of DMA controller) comprising:

a first register (see item 25 in figure 2) for permitting a CPU to make for DMA transfer therein, the first register capable of storing data (see lines 6-33 of column 4);

an operation register (see item 24 in figure 2) for permitting data stored in the setting register to be written thereto, or an operation counter for performing counting operation by use of the data (see lines 6-33 of column 4);

an operation controller (see item 22 in figure 2) for performing control so that, when DMA transfer is started, the data stored in the setting register is written to the operation register or the operation counter (see lines 33-60 of column 4); and

a transfer executer (see item 23 in figure 2) for executing DMA transfer based on the data stored in the operation register or the operation counter (see lines 33-60 of column 4).

8. Referring to claim 7, Taniai teaches a DMA controller according to claim 2, and further teaches the first register is adapted to make settings for DMA transfer (see lines 6-33 of column 4), and the DMA controller further comprises a second register for permitting data stored in the first register to be written thereto, wherein the operation controller is adapted to perform control so that, when DMA transfer is started, the data stored in the first register is written to the second register, and wherein the transfer executer is adapted to execute the DMA transfer based on the data stored in the second register (see

lines 33-50 of column 4, note the information in the NEXTS register is used for setting up the next transfer when the current transfer is executing

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taniai in view of Sato et al. (U.S. Patent No. 5,640,598 hereinafter "Sato").

11. Referring to claim 8 and 9, Taniai teaches the DMA controller of claim 2, but fails to teach a third register and fourth registers for permitting the CPU to make DMA transfer therein and register being capable of storing data; a second operation counter for performing counting operation by use of the data stored in the third register; and a second operation controller for performing control so that, when DMA transfer is started, an occurrence of data storage in the third register is

counted by the second operation counter, wherein the transfer executer is adapted to execute DMA transfer based on the first and second operation counters.

Sato teaches, in an analogous system, the above limitation (see lines 33-67 of column 5).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Taniai with the above teachings of Sato. One of ordinary skill in the art would have been motivated to make such modification in order to reduce command processing time by storing the transfer instructions in advance as suggested by Sato (see lines 9-27 of column 6).

12. Claims 3 and 6,8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taniai in view of Sato et al. (U.S. Patent No. 5,640,598 hereinafter "Sato") and further in view of Hoshino (JP 02195464 A).

13. Referring to claims 3 and 6, Taniai teaches a data processing apparatus (figure 1) comprising a CPU (see item 10, figure 1) for executing a program and a memory (item 14, figure 1) for storing data or for storing data and the program wherein the data can be read out from the memory through a DMA

controller (item 11, figure 1), the DMA controller (see figure 2 for block diagram of DMA controller) comprising:

a setting register (see item 25 in figure 2) for permitting a CPU to make settings for DMA transfer therein (see lines 6-33 of column 4);

an operation register (see item 24 in figure 2) for permitting data stored in the setting register to be written thereto, or an operation counter for performing counting operation by use of the data (see lines 6-33 of column 4);

an operation controller (see item 22 in figure 2) for performing control so that, when DMA transfer is started, the data stored in the setting register is written to the operation register or the operation counter (see lines 33-60 of column 4); and

a transfer executer (see item 23 in figure 2) for executing DMA transfer based on the data stored in the operation register or the operation counter (see lines 33-60 of column 4).

Taniai fails to teach the limitation of a setting execution register for storing transfer conditions under which to transfer, by DMA transfer, transfer conditions for DMA transfer from an external memory to the setting register.

Sato teaches, in an analogous system, the above limitation (see lines 9-27 of column 6).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Taniai with the above teachings of Sato. One of ordinary skill in the art would have been motivated to make such modification in order to reduce command processing time by storing the transfer instructions in advance as suggested by Sato (see lines 9-27 of column 6).

The combination of Taniai and Sato fails to teach the limitations of a selector for alternatively selecting one of the setting register and the setting execution register; a selection controller for performing control so that the register selected by the selector is switched alternately between the setting register and the setting execution register every time DMA transfer ends.

Hoshino teaches, in an analogous system, the above limitation (see abstract).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Taniai and Sato with the above teachings of Hoshino. One of ordinary skill in the art would have been motivated to make such modification in order to omit initialization in each transfer and increase transfer speed by

providing the equipment with files for storing various kinds of transfer conditions as suggested by Hoshino (see abstract).

Response to Arguments

14. Applicant's arguments filed 10/2/06 have been fully considered but they are not persuasive. The applicant argues:

1) Taniai fails to teach or suggest an operation counter for performing a counting operation by use of data stored in a first register (see first full paragraph of page 9).

2) Taniai fails to teach "an operation register for storing transfer conditions under which DMA transfer is to be executed next time," as required by claim 3 (see first full paragraph of page 10);

3) The Examiner is relying on the same element of Taniai to teach both the operation controller of claims 2 and 5 and the operation register controller of claims 3 and 6 (see last full paragraph of page 10);

4) Hoshino teaches a selector, however fails to teach the selector selecting between a setting register and a setting execution register (see second full paragraph of page 11).

As per argument 1, the Examiner disagrees. Taniai does teach a counter for performing count operations and teaches the counter

is initialized by stored data and renewed by the ALU (see 32-38 of column 4).

As per argument 2, the Examiner disagrees. There is no such limitation in claim 3 that recites "an operation register for storing transfer conditions under which DMA transfer is to be executed next time." The claim requires "an operation register for storing transfer conditions under which DMA transfer is currently executing (see claim 3, lines 2-3). This limitation is taught by Taniai at the cited portions of the disclosure.

As per argument 3, claims 2 and 3 are separate independent claims therefore there is no conflict by the Examiner relying on an element from Taniai to teach a limitation from claim 2 and a limitation from claim 3, especially when the limitations are similar. For example, claim 2 requires an operation controller write data to a register when a DMA transfer is started and claim 3 requires an operation register controller for writing to a register when a DMA transfer is started.

In response to applicant's arguments against the references individually (argument 4), one cannot show nonobviousness by attacking references individually where the rejections are based

on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Taniai and Sato are relied upon to show the setting register and setting execution register. Hoshino is relied upon to teach a selector selecting between two registers.

As per arguments 1-4, it is noted that the claims include intended use recitations. For example "a register ***for permitting...***" or "an operation counter ***for counting...***". A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. Per MPEP 2114, "While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); see also In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971); In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959)."

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J. Sorrell whose telephone number is 571 272-4160. The examiner can normally be reached on Monday-Friday 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EJS
December 22, 2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER
12/22/06